



# IP Datasheet

StreamDSP LLC  
1275 Kinnear Rd  
Columbus, OH 43212 USA (855) DSP-FPGA  
<http://www.streamdsp.com>  
email: [sales@streamdsp.com](mailto:sales@streamdsp.com)

## Serial FPDP for Altera and Xilinx FPGAs

Serial Front Panel Data Port is an industry standard, low-overhead, low-latency, high speed serial communications protocol. sFPDP is ideal for use in applications such as high-speed communication system backplanes, high-bandwidth remote sensor systems, signal processing, data recording, and high-bandwidth video systems. The simple and lightweight nature of the protocol makes it an attractive choice for replacement of parallel bus interconnects using serial transceiver technology. sFPDP can be used in point-to-point or loop topologies, uni-directional or bi-directional links, and easily supports different types of data with efficient and flexible data framing options.

StreamDSP is committed to performance, efficiency, and flexibility. Our sFPDP core is unique in that we support nearly all transceiver based devices from Altera and Xilinx. We're always making improvements to the core with innovative new features such as multi-lane bonding for increased bandwidth, and we're continually updating the core to support new transceiver based devices offered by both Altera and Xilinx. Our core provides a open interface to the FPGA transceiver, giving the user complete control over transceiver speed, settings and adjustments. A complete reference design is provided for each family, as well as a thorough testbench with support for Aldec's Active-HDL and Riviera-Pro as well as Mentor's ModelSim tools. In addition, our testing procedure includes exhaustive Altera <-> Xilinx interoperability testing to ensure compatibility.

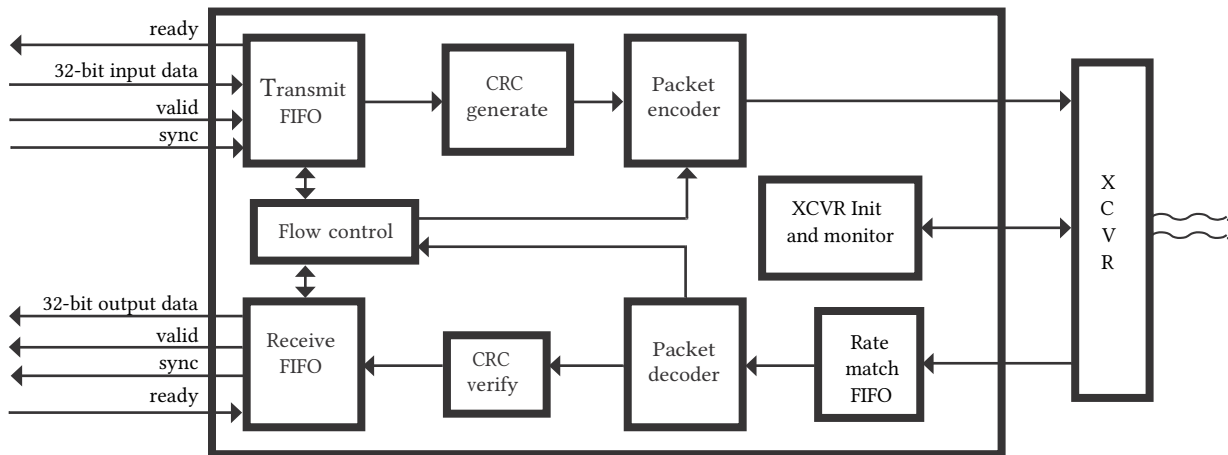
StreamDSP is committed to delivering the highest level of customer support to ensure a smooth system integration. We also offer IP core customization and FPGA design services.

### Features

- VITA 17.1-2003 Compliant
  - Conforms to FC-PH disparity rules
  - Multi-lane channel bonding wrapper
  - Independent data / system clock domains
  - 600 Mbps to 10+ Gbps serial rate support
  - Optional flow control and CRC
  - 32-bit user data interface
  - Basic control/status interface
  - Unidirectional and bidirectional support
  - Optional link startup "junk filtering"
  - All sFPDP frame types supported
- Unframed data
  - Single frame data
  - Fixed size repeating frame data
  - Dynamic size repeating frame data
    - All sFPDP system configurations
      - Basic System
      - Flow Control
      - Bidirectional Data Flow
      - Copy Mode
      - Copy/Loop Mode

## Details

StreamDSP LLC  
 1275 Kinnear Rd  
 Columbus, OH 43212 USA (855) DSP-FPGA  
<http://www.streamdsp.com>  
 email: sales@streamdsp.com



### Resource Usage

Registers	LUTs	*RAM
772	841	14 Blocks

\* RAM size dependent on user controlled TX and RX FIFO depths

### Throughput (per lane)

Line Rate	Throughput
2.5 Gbps	247 MB/s
4.25 Gbps	420 MB/s
5.0 Gbps	494 MB/s
6.375 Gbps	630 MB/s
8.5 Gbps	841 MB/s
10.0 Gbps	990 MB/s

### Delivery Options

HDL Language: VHDL

License Types:

- Netlist
- Source Code

\* Free, supported evaluations available on request

### FPGA Family Support

#### ALTERA

- Cyclone-IV GX
- Arria GX
- Arria-II GX
- Arria-V GX
- Stratix-II GX
- Stratix-IV GX
- Stratix-V GX

#### XILINX

- Spartan-6 LXT
- Kintex-7
- Virtex-4 FX
- Virtex-5 LXT
- Virtex-5 FXT
- Virtex-6 LXT
- Virtex-7

#### Example Design

Altera Cyclone-IV GX Starter Kit  
 Altera Arria-GX PCIe Dev Kit  
 Altera Arria-II GX PCIe Dev Kit  
 Altera Arria-V GX PCIe Dev Kit  
 Altera Stratix-II GX PCIe Dev Kit  
 Altera Stratix-IV GX PCIe Dev Kit  
 Altera Stratix-V GX PCIe Dev Kit

Xilinx SP605 Development Kit  
 Xilinx KC705 Evaluation Kit  
 Xilinx ML405 Development Kit  
 Xilinx ML555 Development Kit  
 Xilinx ML507 Development Kit  
 Xilinx ML605 Development Kit  
 Xilinx VC707 Evaluation Kit

All deliveries include VHDL and Verilog simulation models, a self-checking testbench with simulation scripts, and ready-to-run design targeted at a popular development board for each family (listed above).